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TRENDS AND TECHNIQUES

FOR

SPACE BASE ELECTRONICS

(NASA-CR-161277) A STUDY OF TRENDS AND
TECHNIQUES FOR SPACE BASE ELECTRONICS
Quarterly Progress Report, 11 Jun. - 10 Sep.
1978 (Mississippi State Univ., Mississippi
State.) 38 p HC A03/MF A01

N81-12327

CSCL 09C G3/33 29239

Unclass

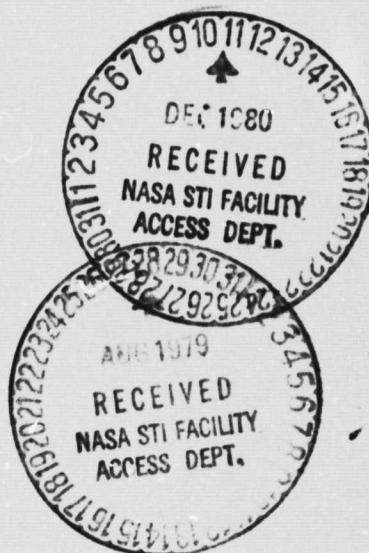
Prepared for

George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama 35812

by

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T.E. Wade
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QUARTERLY REPORT

June 11, 1978 - September 10, 1978

CONTRACT NAS8-26749

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TECHNICAL REPORT STANDARD TITLE PAGE			
1. REPORT NO.	2. GOVERNMENT ACCESSION NO.	3. RECIPIENT'S CATALOG NO.	
4. TITLE AND SUBTITLE		5. REPORT DATE	
A STUDY OF TRENDS AND TECHNIQUES FOR SPACE BASE ELECTRONICS		September 1978	
6. PERFORMING ORGANIZATION NAME AND ADDRESS		7. PERFORMING ORGANIZATION REPORT NO.	
Department of Electrical Engineering Mississippi State University Mississippi State, MS. 39762		MSU-EE-QUAR-4-78	
8. SPONSORING AGENCY NAME AND ADDRESS		9. WORK UNIT NO.	
National Aeronautics & Space Administration Washington, D.C. 20546		NAS8-26749	
10. SPONSORING AGENCY CODE		11. CONTRACT OR GRANT NO.	
12. SPONSORING AGENCY CODE		13. TYPE OF REPORT & PERIOD COVERED	
14. SPONSORING AGENCY CODE		Quarterly Progress	
15. SPONSORING AGENCY CODE		June 11 - September 10, 1978	
16. SUPPLEMENTARY NOTES			
Prepared by Mississippi State University for George C. Marshall Space Flight Center, Marshall Space Flight Center, Alabama			
17. ABSTRACT			
<p>During this second quarter, three activities were in progress: (1) the set-up of furnaces and photolithography related equipment at MSU, (J.D. Gassaway); (2) experiments on double layer metal at NASA/Huntsville (T.E. Wade); and (3) two dimensional modelling of MOSFETS (Q. Mahmood & J.D. Trotter).</p> <p>The MSU I.C. Laboratory has in place the furnaces, the photolithography facilities and metallization system to reproduce the NASA/Huntsville double layer metal process - the only missing equipment being the SiO₂ vapox reactor. Two Pacific Western units are in the process of being donated to MSU by Synertek.</p> <p>The double layer metal activity initially emphasized wet chemistry techniques. By incorporating the following techniques: (1) ultrasonic etching of the vias, (2) premetal clean using a modified buffered HF, (3) phosphorus doped vapox, and (4) extended sintering, yields of 98% were obtained using the standard test pattern.</p> <p>The two dimensional modelling activity is in the middle of development. Principle problems have stemmed from alternately, instability and too much computation time to achieve convergence. Modifications are in progress.</p>			
18. KEY WORDS		19. DISTRIBUTION STATEMENT	
Multi-level metal processes Double layer metal Sintering effects Integrated circuit technology Aluminum metallization			
20. SECURITY CLASSIF. (of this report)		21. NO. OF PAGES	
Unclassified		22. PRICE	
20. SECURITY CLASSIF. (of this page)			
Unclassified			

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A. DOUBLE LAYER METAL SINTERING EFFECTS

AI. INTRODUCTION

The increasing demands toward greater packing densities in LSI and VLSI make it imperative that multilevel metallization systems be developed. Although several reviews have been written ¹⁻⁷, the realization of reproducible and reliable results have yet to be forthcoming. The most common problem associated with double layer metal has been the inability to make electrical contacts between metal layers through via holes etched in the dielectric to provide electrical communication between metals. The problem is more acute when the number of vias is large (>500) and are relatively small in size (<0.2 mil square). Another, less important problem is associated with shorts between metal layers due to pinholes in the dielectric film, thin spots, or poor coverage of hillocks in the first level metal. An example of the use of double layer metal for circuit application ⁸ is given in Figure 1.

In order to study the effects associated with double layer metal structures having a large number of small vias, a test pattern was generated consisting of a string of 560 vias. The via size was varied from 0.5 mil square to 0.2 mil square per string. Electrical measurements were made on the test pattern after initial sintering and subsequent heat treatments in order to monitor contact resistance behavior and variations in yield. Metal interconnects between vias were typically 0.7 mils wide although samples were also prepared and tested having interconnects of 0.4, 0.5, and 0.6 mil wide Al, with little or no variation in results.

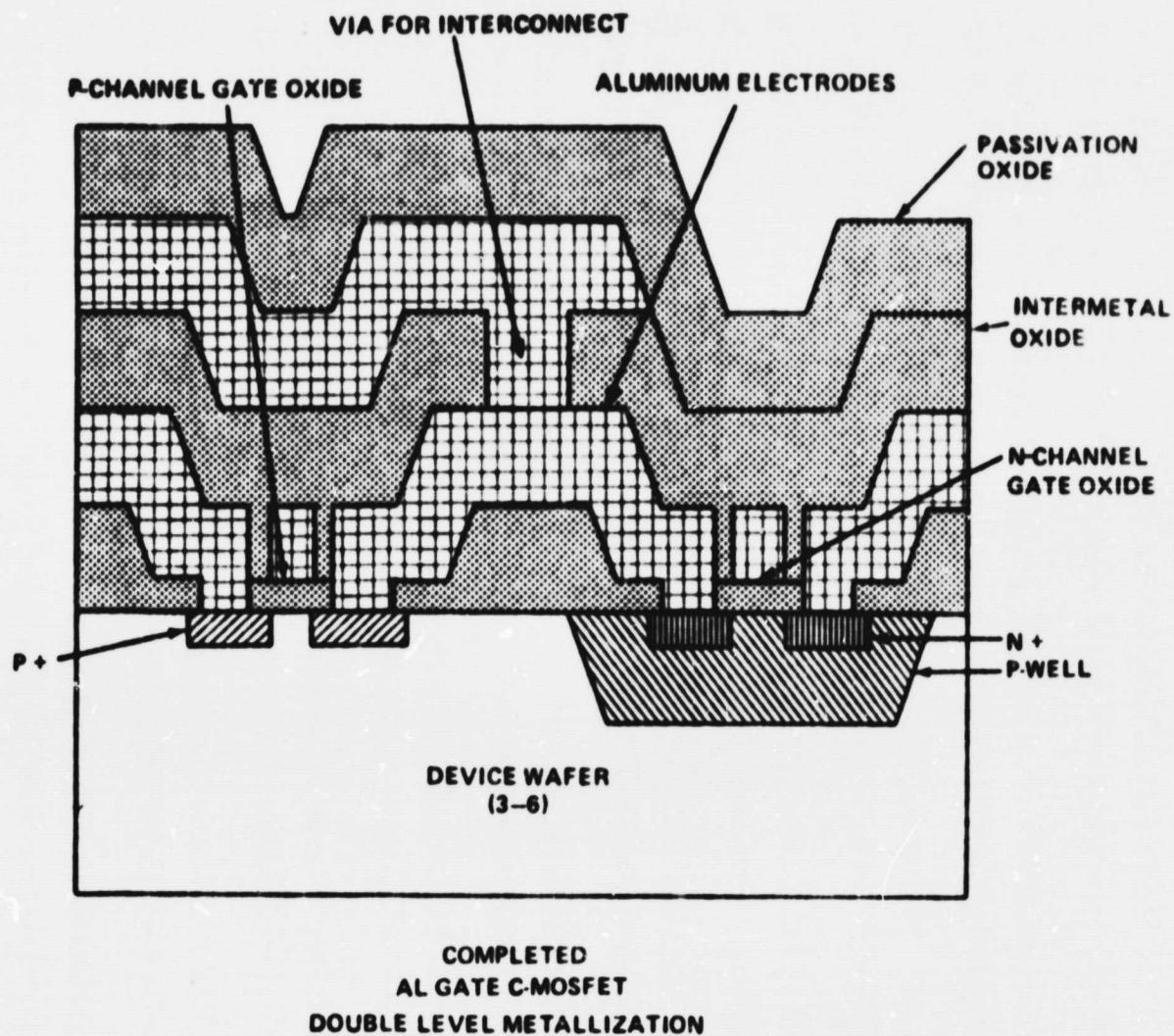


Figure 1. An example of the use of double layer metal in the realization of an aluminum gate C-MOSFET structure.

III. PREPARATION OF TEST VEHICLE

The steps involved in preparing the test vehicle consist of the following. The starting material was 3-8 ohm-cm, (100) oriented, n-type phosphorous doped silicon wafers. A field oxide was thermally grown in dry O_2 for 5 minutes, boiling H_2O for 60 minutes and then dry O_2 for an additional 15 minutes at 900°C resulting in an oxide thickness of $14\text{ }^{\text{\AA}}$. Prior to depositing the first layer metal, a cleaning step was performed, this consisted of a one-minute dip in dilute HF: H_2O (1:10) at room temperature and a 10 minute rinse in deionized water. The wafer was then dehydrated at 900°C in an N_2 ambient for 10 minutes. The first metal layer was d.c. sputtered structural grade Al alloy 6061 of $0.5\mu\text{m}$ thickness. The metal was patterned using conventional photolithographic techniques with Waycoat-31 negative photoresist.

Prior to depositing the dielectric, scribe lines (0.7 mils wide) were etched around the test patterns through the thermally grown field oxide down to the silicon substrate. These lines were used as an etch end-point monitor in etching vias in the intermetal dielectric.

The intermetal oxide was next deposited at 400°C using CVD of SiH_4 (4% in Ar) and O_2 (and later P_2O_5 of approximately 3 mole percent) to a thickness of $8\text{ }^{\text{\AA}}$. Dielectric thickness was measured with an (laser) ellipsometer. Vias were etched in this dielectric film with buffered HF using standard photolithographic masking. This etching was done first by dipping the wafers in a stirred

solution of etchant, using the scribe lines as reference to determine when etching was completely through the dielectric film. In later processes, this etching was done ultrasonically in a totally enclosed container.

The second layer metal was also deposited using dc sputtering of the same target used in the first layer metal and patterned. Typically a 15 minute aluminum sintering process at 470°C preceded the first testing of the completed test vehicle.

AIII. EXPERIMENTAL RESULTS

Approximately 50 wafers were processed. Each wafer had 200-220 test patterns with via sizes ranging from 0.2 mils square to 0.5 mils square. Table I represents a summary of results in terms of percent yield obtained for each via size as a function of fabrication process. Process A through L are explained below. Among other variables it will be noted that each process is characterized by an etch time associated with etching the vias in the intermetal dielectric film. The scribe lines were used as reference. When all dielectric was etched from these scribe lines, this was defined as the 'break' time. Any additional etching beyond this break time is measured in seconds.

Process Definitions:

A. Wafers were processed as described in section II. The width of the first level metal interconnect of 0.4, 0.5, 0.6 and 0.7 mils corresponded to test patterns having square vias of 0.2, 0.3, 0.4 and 0.5 mils, respectively. The width of the second metal

Via Size	Percentage Yield Via Resistance for 560 Vias < 20 Meg Ohm Process Identification											
	A	B	C	D	E	F	G	H	I	J	K	L
0.5 mils	81	76	95	98	99	98	94	84	94	93	98	98
0.4 mils	70	56	88	94	97	98	92	82	89	90	97	97
0.3 mils	61	53	64	85	93	94	92	83	87	80	100	100
0.2 mils	40	18	64	82	91	94	93	89	72	67	98	98

Table I-A

Via Size	Percentage Yield Via Resistance for 560 Vias < 10 Kil Ohms Process Identification											
	A	B	C	D	E	F	G	H	I	J	K	L
0.5 mils	17	59	86	97	97	94	84	61	92	93	98	98
0.4 mils	8	48	73	89	94	96	88	64	82	90	97	97
0.3 mils	0	30	45	64	89	92	88	74	85	80	100	100
0.2 mils	0	14	13	26	44	59	64	52	38	67	98	98

Table I-B

Via Size	Percentage Yield Via Resistance for 560 Vias < 1 Kil Ohm Process Identification											
	A	B	C	D	E	F	G	H	I	J	K	L
0.5 mils	0	59	78	85	86	82	74	56	92	92	98	98
0.4 mils	0	46	47	66	72	72	68	54	82	90	97	97
0.3 mils	0	28	85	36	47	55	58	56	85	80	100	100
0.2 mils	0	8	10	15	22	27	30	30	32	67	75	98

Table I-C

Table I Percentage yield as a function of processing with via size as a parameter for contact resistance of 560 vias less than 20 Megohm, 10 Kilohm, and 1 Kilohm for tables I-A, I-B, and I-C, respectively.

was 0.7 mils. Via etch time was break plus 10 seconds.

B. Wafers were processed as described in section II. The metal interconnects on both levels were 0.7 mils wide. (This is true for all processes B through H). Via etch time was break plus 10 seconds.

C. Wafers processed as described in section II with via etch time in stirred dielectric etchant extended 20 seconds beyond break time.

D. thru H. correspond to wafers processed as described in section II but with via etch time in stirred dielectric etchant extended 40, 60, 80, 100 and 120 seconds beyond break, respectively. (Note that the values given for processes A through H represent an average of five different process runs of eight wafers for each run.)

I. Wafers processed as described in section II but having a phosphorous doped intermetal dielectric of 3.1 mole percent (as determined by Auger spectroscopy) and with vias etched in stirred dielectric etchant for 20 seconds beyond break.

J. Wafers processed as described in I above except via etching was done ultrasonically in a closed container for 20 seconds beyond break.

K. Wafers processed as described in J above with the addition of a first level metal cleaning step through the vias prior to depositing the second level metal. The metal cleaning solution consisted of an ethylene glycol-buffered HF-H₂O solution for the removal of Al₂O₃ from the first level metal prior to deposition of second level metal¹⁰.

L. Wafers processed as described in K above but having undergone a one-half hour post heat (sintering) treatment at 490°C.

The results of processes C through H are displayed graphically in Figure 2. The data are shown in Tables IA, B, and C which give the percent yield for via contact resistances less than 20 meg-ohms, 10 kil-ohms and 1 kil-ohm. It is desirable to have minimum contact resistance (i.e. less than 250 ohms) since as the number of vias increase from 600 to approximately 3000 for a VLSI circuit, the resistance will increase proportionately. Any pattern having a contact resistance greater than 20 meg-ohm is assumed to be an open-circuit in Table I.

Wafers processed as described in D in Table I were used for an Auger surface analysis of the first level metal through a 0.5 mil via just prior to depositing the second level metal. The purpose of the Auger analysis was to determine what insulating materials reside on the surface of the first level metal which prevented good low resistance ohmic contact between metal levels. The results of this analysis indicated the following materials were present with an accuracy of \pm 5%:

Al_2O_3	64%
C	31%
N	1.8%
Mg	1.3%
Si	0.6%
F	0.6%
S	0.7%
O (other than Al_2O_3)	<0.1%

For this contact, the amounts of Mg and Si were about the same as

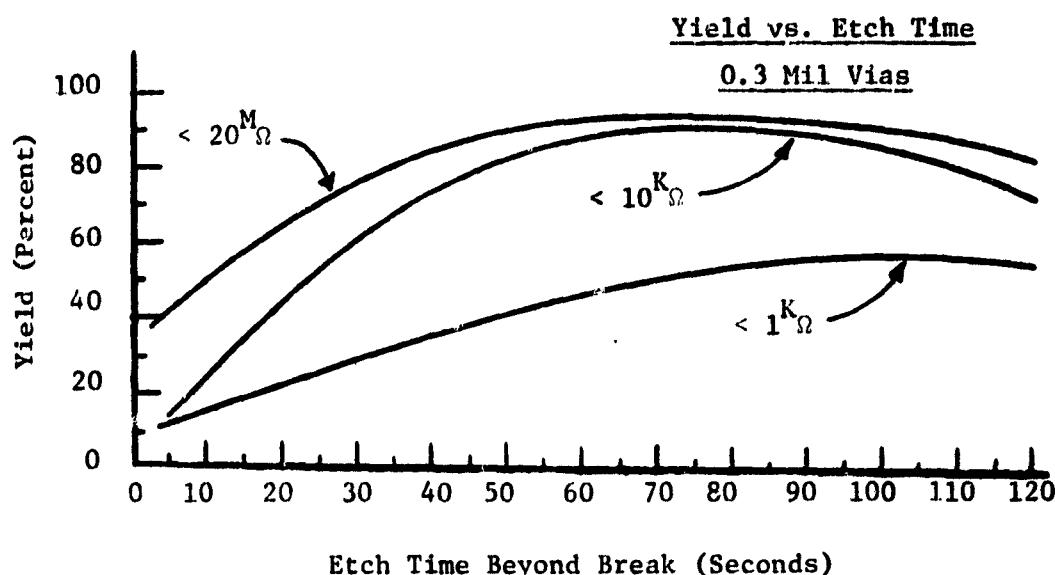
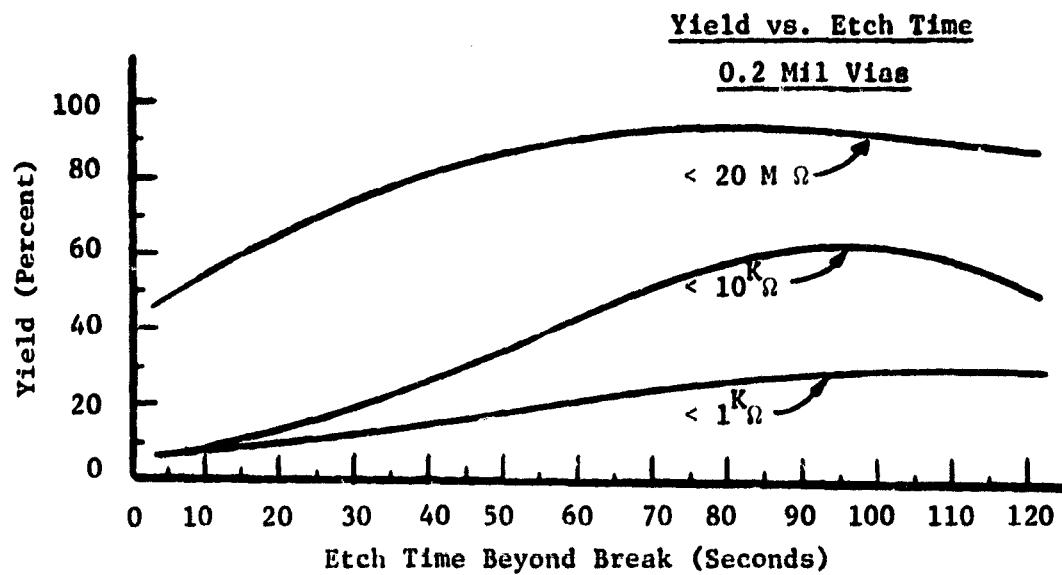


Figure 2. Percent yield as a function of etch time beyond break with via size as a parameter. Intermetal dielectric etch accomplished with stirred B.O.E.

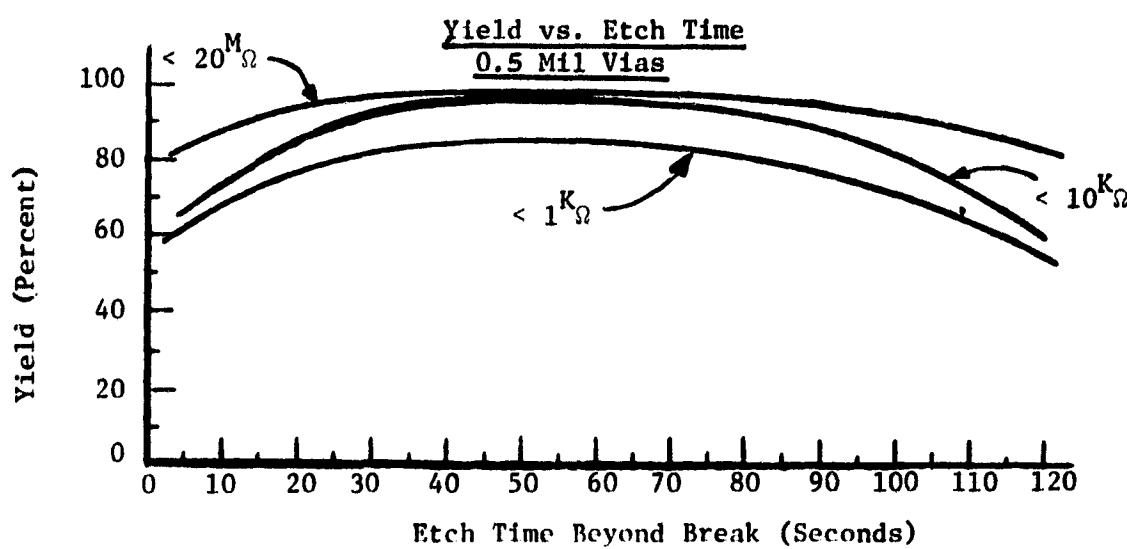
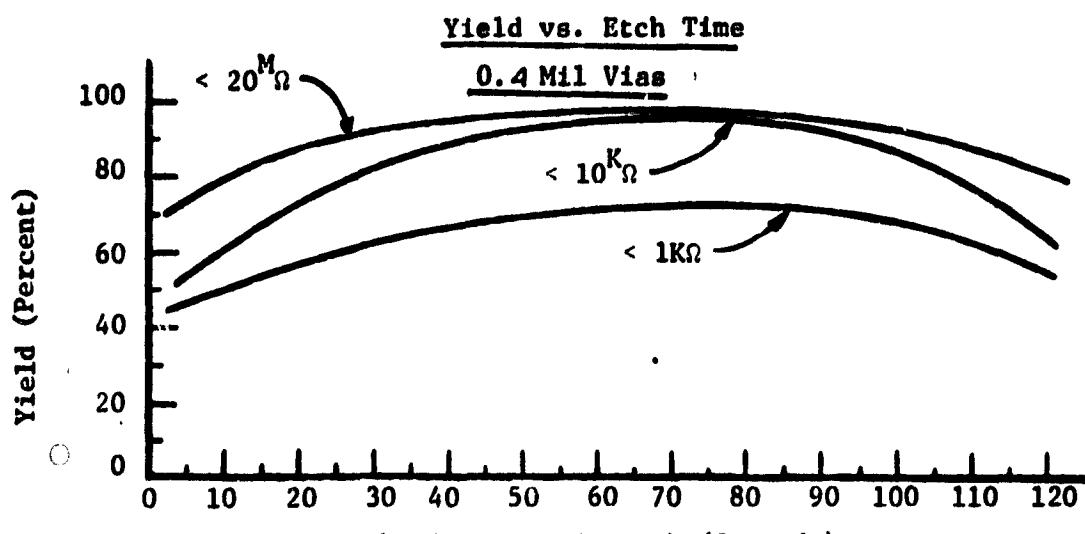


Figure 2. (continued). Percent yield as a function of etch time beyond break with via size as a parameter.
Intermetal dielectric etch accomplished with stirred B. O. E.

the bulk Al alloy so there did not seem to be any surface enrichment of Mg_2Si which was suspected as a source of the high resistance. When about 100\AA of this surface was removed by ion etching, the N, S, F, and C were greatly reduced, which suggested that they may be a source of interfacial contamination.

The large percentage of carbon measured (31%) is believed to be a result of the photoresist leaving a carbon residue on the wafer. The composition of this photoresist could not be obtained from the manufacturer.

It should be noted that the composition of the structural grade Al 6061 consist of the following impurities:

Si	0.4 - 0.8%
Cu	0.15 - 0.4%
Fe	0.7%
Mg	0.8 - 1.2%
Mn	0.15%
Cr	0.15 - 0.35%
Zn	0.25%
Ti	0.15%

The primary reason for using this Al alloy was for the prevention of hillock formation.

Post heat treatment or sintering of a wafer exhibiting an initial poor yield (i.e. less than one kil-ohm for a chain of 560 vias in series) can increase the effective yield by 500 to 700% as illustrated in Figure 3 for wafers 10H and 2W. These wafers were processed as in 'C' above, having only a 15 minute 470°C sintering before initial testing. All addition sintering was done at 490°C in a nitrogen ambient.

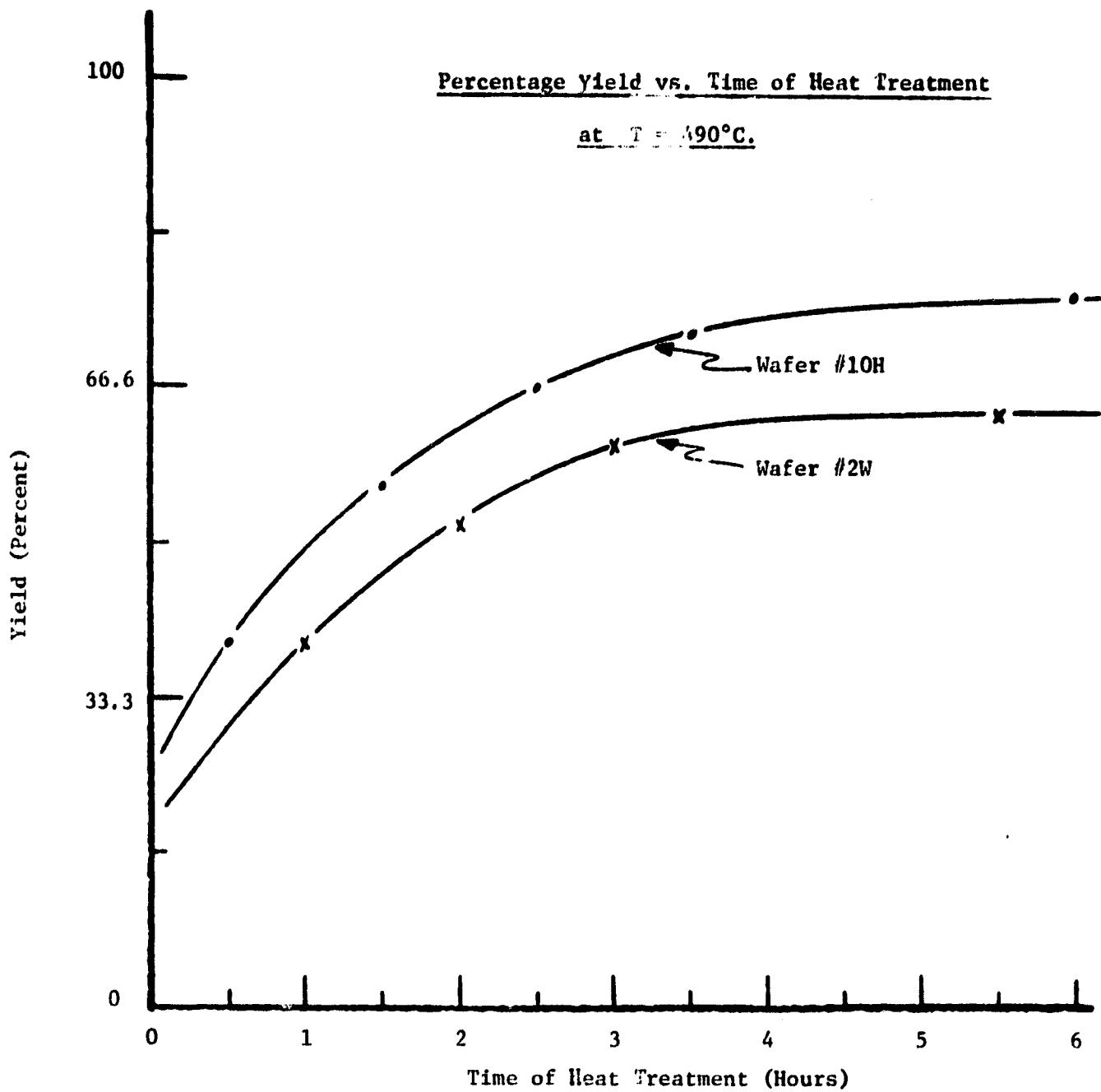


Figure 3. Percentage yield of number of chips less than 1 kil ohm as a function time of heat treatment at 490°C for wafers with undoped intermetal dielectric.

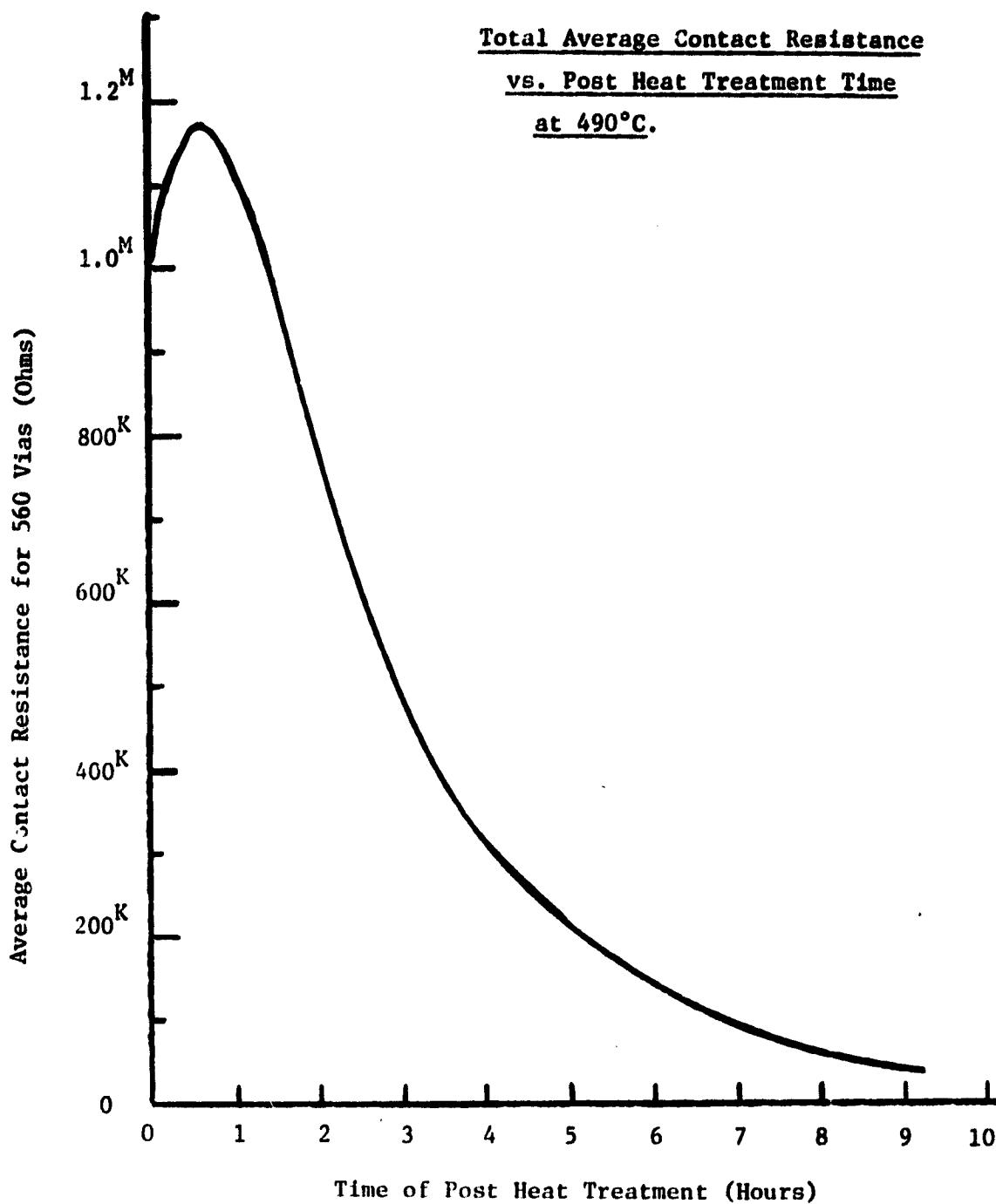


Figure 4. Average contact resistance for 560 vias of all 0.5 mil square chips as a function of post heat treatment time for wafer #2W. (Total number of chips = 55)

The primary reason for this increase in yield with post heat treatment is due to the fact that the Al-to-Al contact resistance decreases with sintering, as demonstrated in Figure 4. Here, the average resistance for all test patterns having 0.5 mil square vias (approximately 55 of the total 212 chips) is plotted as a function of sintering time. As the time of sintering increases, the number of test patterns having a contact resistance < 1 kil-ohm increases, hence the yield increases.

On an individual chip basis, the contact resistance for 560 vias per chip behaved as shown in Figure 5. For a given wafer which initially exhibits a relatively poor yield, the number of chips behaving in the manner shown for chips #10C and 10W was approximately 51%, those behaving like chip #10R was 27% and those like chip #10T was 10%. The remaining chips either exhibited low initial contact resistance (<300 ohms) or were open-circuited (>20 meg-ohms). Those chips initially exhibiting a low contact resistance generally had their resistance lowered with increasing heat treatment, however a few chips showed a gradual increase in resistance with increased heat treatment time as shown in Figure 6. It is believed that this increase in resistance is due primarily to the consumption of Al by SiO_2 to lessen the Al thickness. Since at 490°C Al reacts chemically with SiO_2 to form Al_2O_3 and free Si, Al is consumed at a rate of $210\text{\AA}/\text{hr}$.¹⁵

The most predominant trend found in sintering of double level metal test patterns is demonstrated in Figure 7. As inferred

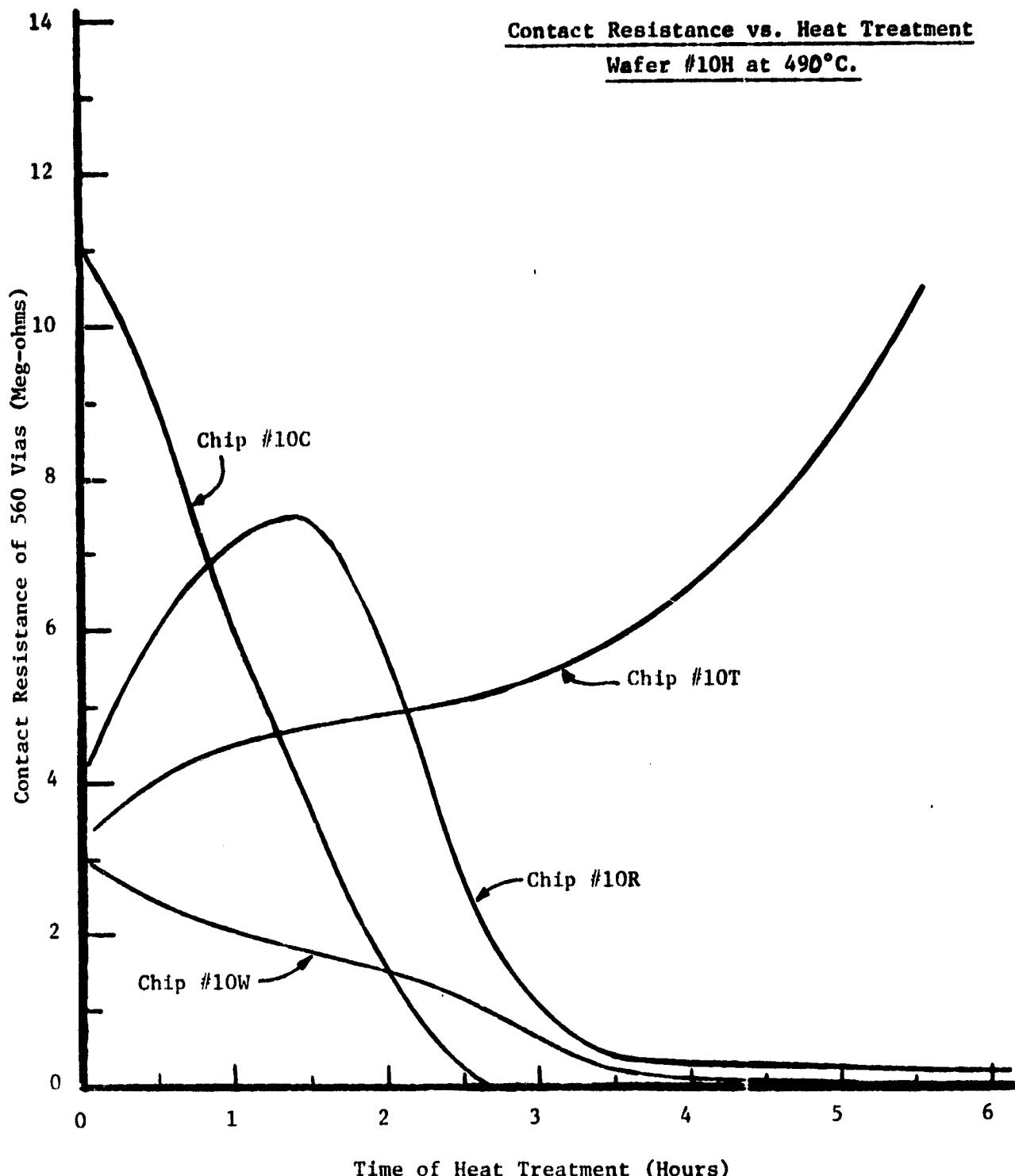


Figure 5. Contact resistance of 560 vias as a function of heat treatment time for several different chips of wafer #10H at a temperature of 490°C.

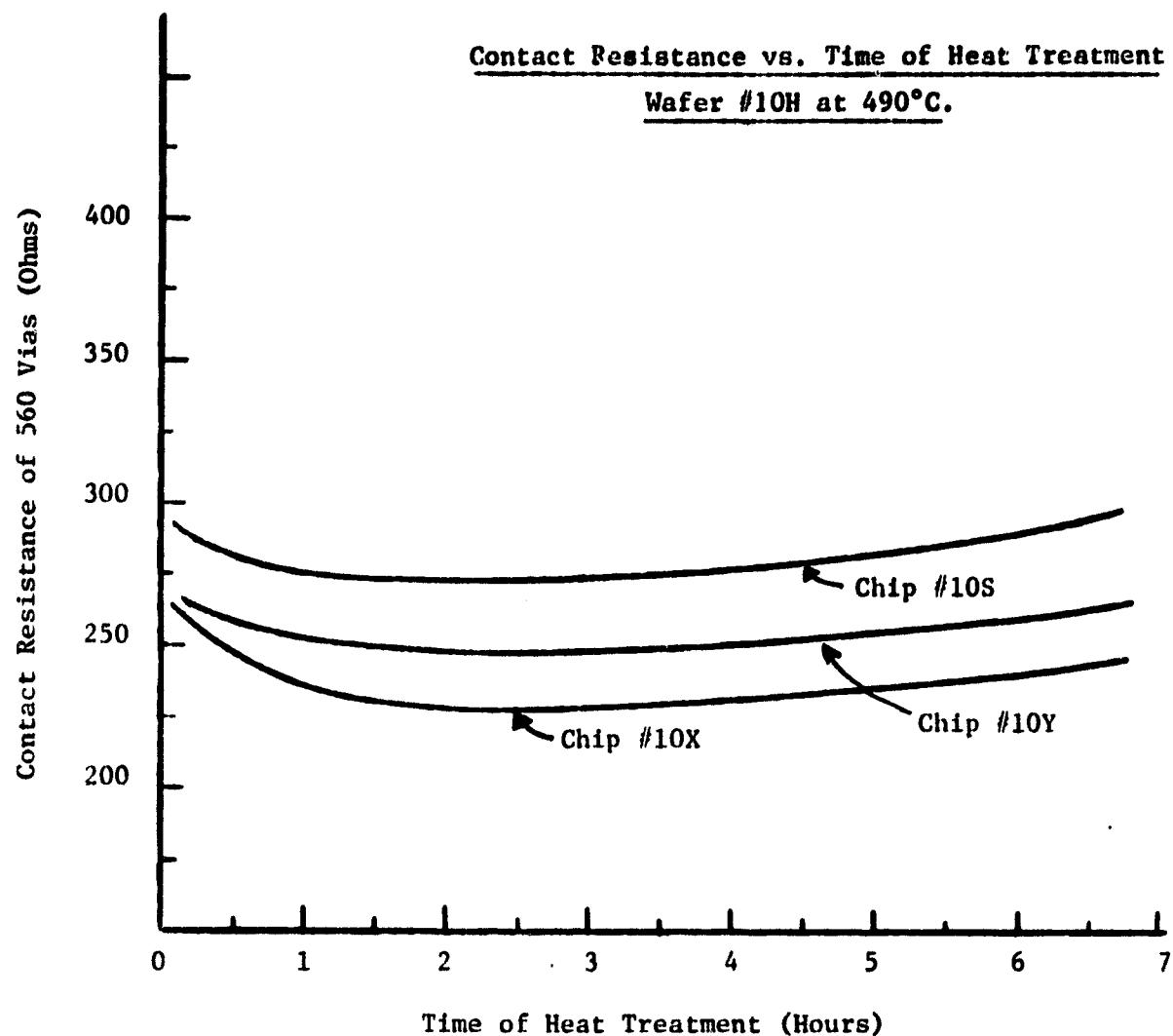


Figure 6. Contact resistance of 560 vias as a function of heat treatment time for wafer #10H showing slight increase in resistance with time of heat treatment for ~6% of the chips on the wafer.

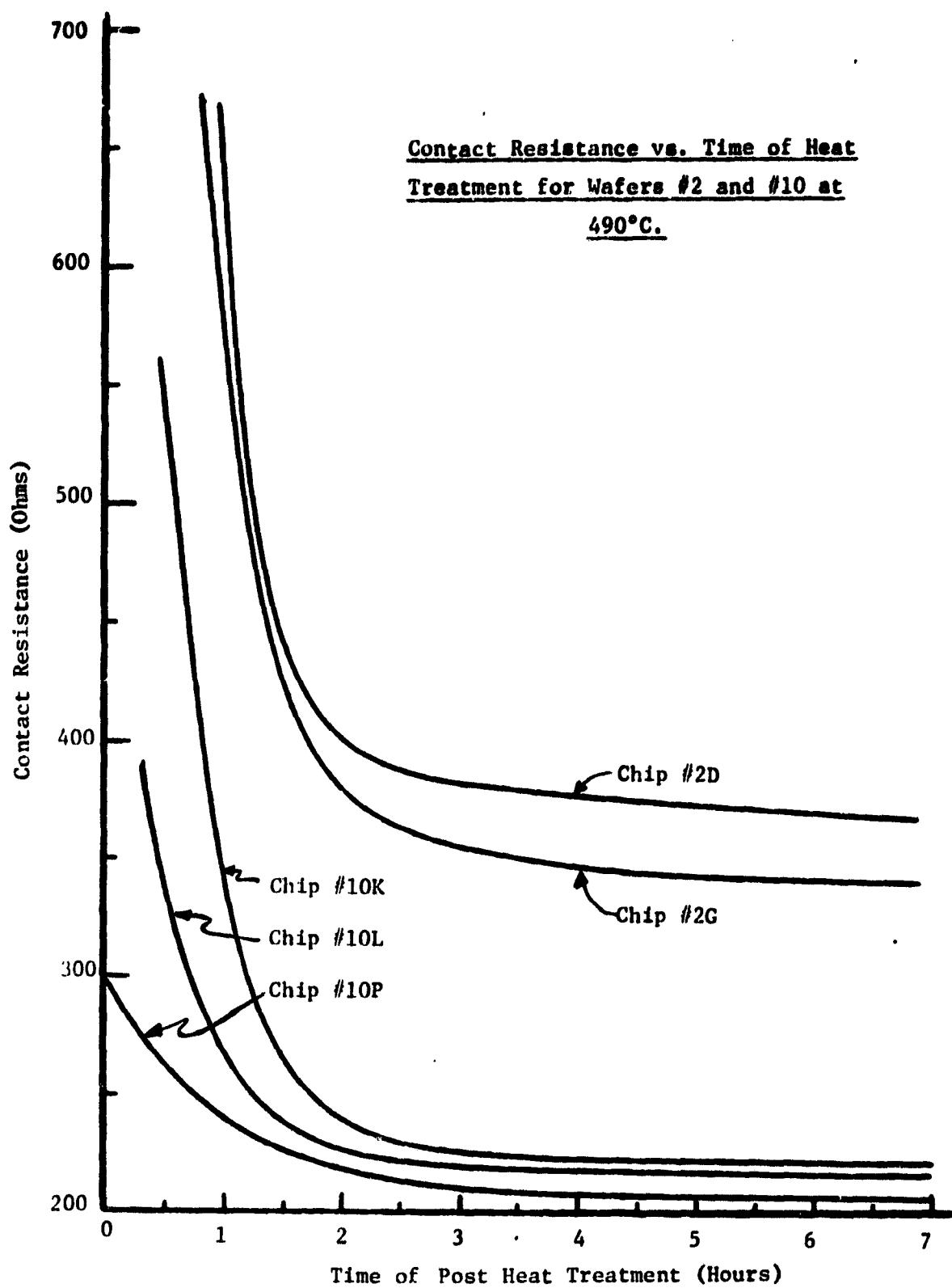


Figure 7. Contact resistance trends as a function of heat treatment time for wafers #2 and #10.

from this plot of contact resistance as a function of post-heat treatment for these two wafers, the average contact resistance decreases drastically for the first few hours of sintering. Because of this feature, the realization of multiple level metal LSI having a large number of vias (>2000) is a distinct possibility.

One major problem involved in post heat treatment of double layer metal structures is that the dielectric (C.V.D. - SiO_2) has a tendency to crack or "craze" at elevated temperatures (>500°C). This cracking, as illustrated in Figure 8, is due to excess stress on the insulating layer⁹. One method to lessen, if not-alleviate this problem, is to use a phosphorous doped dielectric of 3 to 5 mole percent. This increases the effective temperature for which sintering can be done before cracking is observed⁹.

Using this phosphorous doped dielectric (also called phosphosilicate glass or PSG) resulted in a much higher yield as shown in Table I and also a considerable less contact resistance as shown in Figure 9. Here the average contact resistance as a function of via size is plotted for a test pattern with a doped dielectric layer for no heat treatment (curve B) and with 30 minutes post heat treatment at 490°C (curve A). These results are compared to the best results obtained for the undoped case (curve C), even after many hours of heat treatment. The table in the figure indicates resistance and percent yield for each case presented.

A resistance map of the wafer shown in curve B is given below:

173	159	154	217	161	143	158	196	176							
170	171	~	157	231	158	161	159	183	171	158					
166	163	168	158	166	226	162	162	171	167	161	164				
164	164	167	161	158	208	164	159	161	172	170	163	165	173		
168	170	170	160	159	212	163	161	163	228	169	164	~	172	164	
157	168	169	170	165	158	219	162	161	160	234	168	163	163	170	160
164	170	170	171	164	156	213	161	163	159	221	173	159	163	170	165
112	173	201	176	164	151	143	173	~	163	192	174	162	162	170	171
164	175	375	181	167	159	405	172	162	158	181	167	161	164	167	165
177	202	182	169	159	211	164	161	154	176	164	160	156	166		
176	216	184	171	161	228	169	158	154	~	162	156	154	165		
44	198	179	171	162	228	164	158	153	173	160	157	151			
260	181	171	163	231	166	159	154	172	160	153					
177	166	200	167	159	151	167	157								

Via size .4 .5 .2 .3 .4 .5 .2 .3 .4 .5 .2 .3 .4 .5 .2 .3 .4

IV. ANALYSIS AND CONCLUSIONS

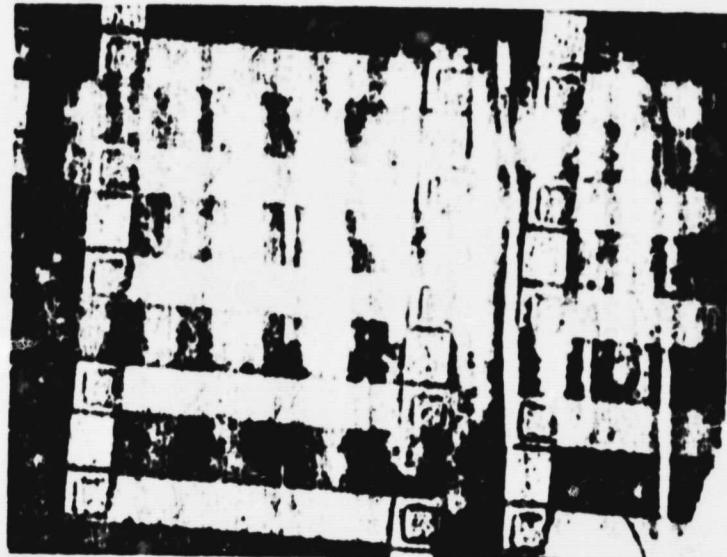
The following comments and conclusions may be derived from this investigation.

1.) The variation in width of the metal interconnects between vias had little influence on yield, as expected. It may have had a slight effect on total resistance, especially for the 0.4 mil compared to 0.7 mil wide interconnect, but this was not detectable. The major difficulty came in mask alignment of the smaller interconnects.

2.) The extension of the via etch time of the dielectric film for both the dipped (stirred) etching and the ultrasonic etching



Photomicrograph (A)



Photomicrograph (B)

Figure 8. Photomicrograph of test pattern at 300X magnification illustrating crazing tendency at temperatures $>500^{\circ}\text{C}$ and for fast pull from the furnace. Photomicrograph (A) shows crazing around a test pad whereas (B) shows crazing in the test pattern itself.

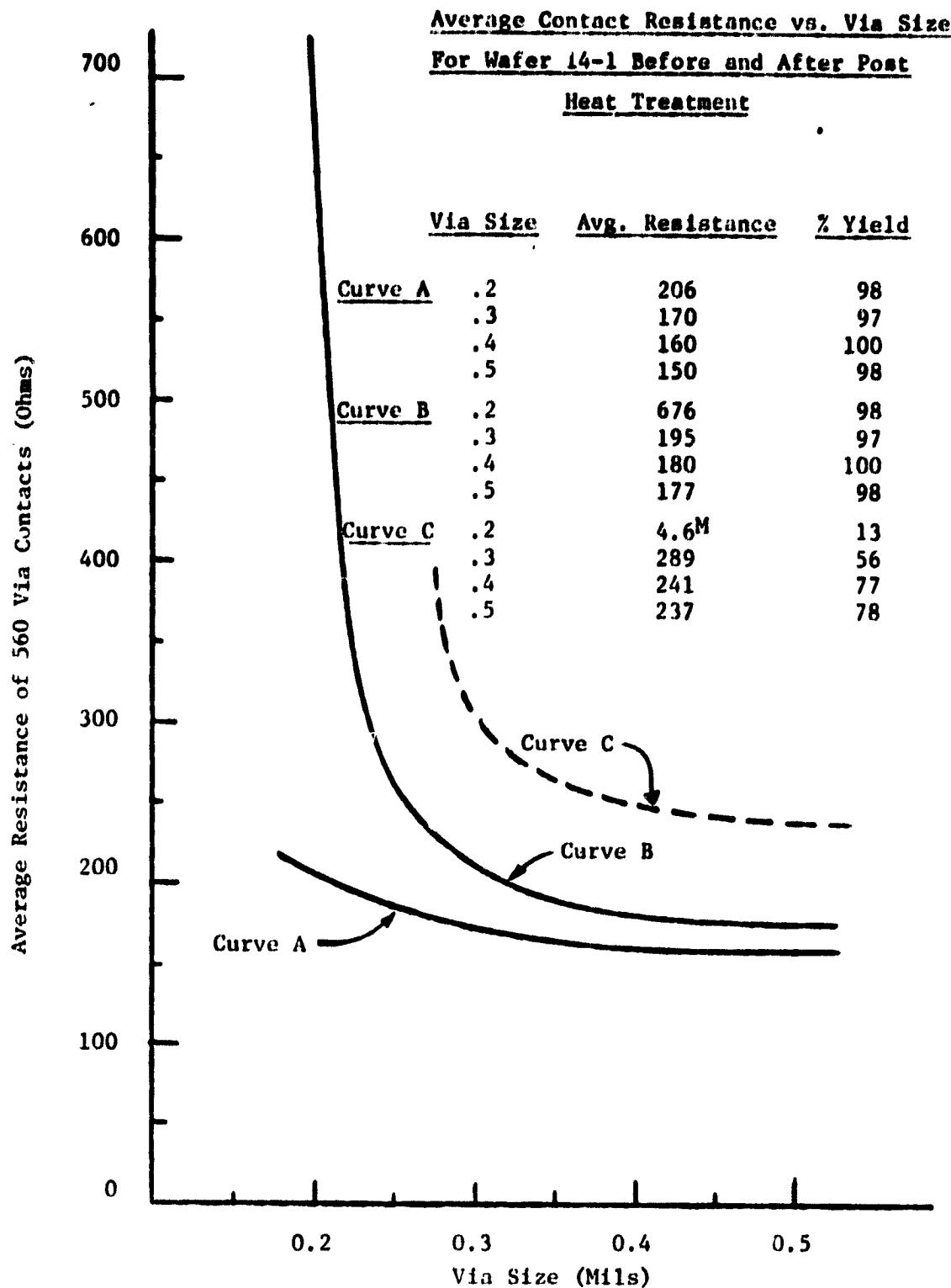


Figure 9. Average contact resistance vs. via size for wafer #14-1 having phosphorous doped intermetal dielectric before post heat treatment (curve B) and after 30 minutes at 490°C (curve A). For comparison with a wafer having an undoped dielectric, curve C represents such a wafer after undergone 8 hours of post heat treatment at 490°C. (Note contact resistance for 0.5 mil via of wafer in curve C prior to post heat treatment was 90 kilohms.)

difficulty of removing all of the dielectric film from the via and the formation of oxides of the alloys contained within the Al all tend toward low yield, high resistance contacts. There are actually two approaches for solving this problem, back sputtering and chemical etching. Back sputtering has the advantage that the oxide thickness can in principle be reduced to zero if the subsequent metallization is applied without exposure to air. The disadvantages include: possibility of radiation induced MOS damage; potential for contamination of the sputtering system; redeposition of previously sputtered materials especially from the substrate table; etc. The chemical etch procedure does not have these disadvantages, but the oxide thickness can never be reduced to zero.¹⁴

The use of a 1:1:1 ethylene glycol: buffered -HF : H₂O etch removes all but 30-50 Å of oxide¹⁰ without attacking the Al. (The second layer sputtered Al can easily penetrate this oxide thickness to form good ohmic contacts.) This etch was done just prior to second level metallization.

6.) The application of post heat treatments can drastically increase yield by lowering total via contact resistance. There are several possible reactions which cou' occur to cause this temperature effect.¹¹ Aluminum could react with aluminum oxide in the film between the layers to form various aluminum suboxides and thus break up the continuous layer of dielectric. Alternately, the recrystallization of aluminum in both of the levels could mechanically disrupt the thin native oxide layer, therefore forming aluminum-to-aluminum contact. As yet, there is no evidence for this

speculation.

Figures 4 and 5 indicate that in some cases the contact resistance increases with post heat treatment time prior to the "diffusion" through this 'interfacial contamination' by the two layers of aluminum. If this contamination were SiO_2 , then it could be seen that there exists excess ionic silicon in the oxide which becomes tied-up upon the application of post heat treatments¹². Since the contamination is probably Al_2O_3 , one might say there exist excess ionized Al in the oxide which reacts with the oxidizing species during the sintering process, thus decreasing the total ionic charge in the oxide layer causing the net resistance to increase.

7.) Testing the via test pattern can be tedious. For high resistance vias the measured resistance was seen to be both light sensitive and current sensitive. As a result, all testing was accomplished in the dark. Ideally, very low testing potentials are applied in order not to break down a barrier layer thus turning a defective via into a good one. Also, theoretically, vias should not be tested in series, since the entire applied voltage will be dropped across a defective via, probably causing it to break down and appear good. However, in our testing, all vias were measured at once in series using a digital voltmeter.

8). Recently, a new planar multilevel interconnection technology was introduced¹³ using polyimide films. Although this procedure appears to be very promising for future applications if taken at face value, it is felt there is still many facets of "magic" associated with it.

B. OTHER DOUBLE LAYER METAL EXPERIMENTS

Reviewing the literature has disclosed many investigations relative to the surface oxidation processes of aluminum, including recent reported results by Bell Lab personnel which directly relates to double layer metal processing. These studies show that the aluminum surface is extremely reactive and grows $Al_2O_3 \cdot nH_2O$ films rapidly in water based solutions to thicknesses which cannot be reduced during the sintering operation. Even the growth rate of Al_2O_3 on Al in air at room temperature is reported to be in the range of 30 \AA° . This compares with the Bell Lab's estimate of 55 \AA° of Al_2O_3 which can marginally be reduced by sintering.

Suspect processing steps are many; however, two stand out: (1) the via etch using buffered etch and (2) the initial oxidation during vapox deposition.

Consequently, three sets of experiments have been started:

1. Experiments aimed at measuring the Al_2O_3/Al interface using auger techniques.
2. Experiments using plasma etch and/or nitride insulation.
3. Experiments using in situ back sputtering.

Only the last experiment has been completed. As was expected, the in situ back sputtering gave much improved results over the standard wet chemistry -- the detail results being published elsewhere.

C. TWO DIMENSIONAL MODELLING OF MOSFET

As outlined in the last report key assumptions have been made in order to simplify the computation time:

1. The mobile majority carriers are included in an infinitesimally thick layer of charge at the Si-SiO₂ interface.
2. The current flow is then described by a one-dimensional equation,

$$i = \frac{KT}{q} \mu_N \left(\frac{\partial \mu_L}{\partial x} s + q \frac{\mu_L}{K_t} E_s s \right), \quad 0 \leq x \leq a,$$

where i and s are channel current and charge per unit channel width, E_s is the tangential interface field and μ_N and μ_L are the mobility factors accounting respectively for gate modulation and hot electron effects.

3. The potential in the depletion region is defined by Poisson's equation with appropriate fixed boundary conditions: a) fixed potential along the source drain and substrate, b) the horizontal component of the electric field under the source and drain and far from the channel is zero, and c) the potential in the channel is defined in conjunction with the current equation above plus the one dimensional Poisson equation in the gate oxide.

Obvious limitations of this approach are associated with avalanche and bulk generated leakage currents - which normally are of secondary concern. Additionally, the mobile sheet charge assumption does not allow punch-thru or subthreshold current modelling; however, it is believed that this can be directly added to the

algorithm at an appropriate time. The assumption of a one-dimensional electric field in the oxide is similar to the gradual channel approximation and, consequently, is of fundamental importance.

The initial algorithm utilized iterative techniques in solving first Poisson's equation and then the current equation in the channel. The initial values of potential inside of the boundaries were set at zero. Long computation times were encountered in solving Poisson's equation and instability occurred when iterating through the current equation.

The basic program has been modified to include the gate oxide region in the solution of the Poisson equation - in order not to be limited by the gradual channel approximation. It should be noted however, that routines based on the gradual channel approximation are being utilized in order to develop the initial conditions for the main two-dimensional algorithm. In addition the program has been simplified by assuming constant channel mobility - a restriction which is to be removed at a later time.

Emphasis is now being made on incorporating the following procedures: 1) Using the gradual channel approximation, calculate the channel node potentials. 2) Using the above with the given boundary conditions and the single dimensional d.c., solve for all the potentials in the oxide. 3) Using the alternating direction implicit method with the Newton-Raphson linearization technique, the Poisson equation is solved in the depletion region. 4) The poisson equation and the current continuity equation are simultaneously solved in the channel region. 5) Repeat 3) but extended through the channel

and oxide regions, again using the two-dimensional techniques.

6) Repeat 4). 7) Repeat 5) and 6) until convergence is achieved.

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QUARTERLY
FINANCIAL REPORT

NASA Contract NAS8-26749

June 1, 1978 - August 31, 1978

Prepared for
George C. Marshall Space Flight Center
Marshall Space Flight Center
Alabama 35812

Submitted by
J.D. Trotter, Principal Investigator
T.E. Wade
J.D. Gassaway

COST ANALYSIS OF RESEARCH PROJECTS

CONTRACT 30-45-0210607-232DATE THIS REPORT June 1, 1978 THROUGH June 30, 1978PROJECT TITLE NASA Contract NAS8-26749

	EXPENDITURES THIS MONTH	EXPENDITURES TO DATE	OUTSTANDING COMMITMENTS	FREE BALANCE	TOTAL PROPOSED BUDGET
A. PERSONNEL SERVICES					
(1) Professional					\$22,806
(2) Graduate Assistants					8,550
(3) Undergraduate Assistants					1,650
(4) Technical					
(5) TOTAL PERSONNEL SERVICES	5,143.00	9,604.20		23,431.80	35,916
B. MATERIALS AND SUPPLIES	1.04	462.23		2,387.77	2,850
C. EQUIPMENT					
D. TRAVEL		123.44			
E. EMPLOYEE BENEFITS	636.97	1,023.85		2,429.55	2,551
F. OTHER (Specify) Computer Service				2,674.15	3,695
COMMUNICATIONS				3,000.00	3,000
G. TOTAL DIRECT EXPENDITURES		90.75		- 90.75	
H. INDIRECT COST 45.0% of A(5)	1,306.08	1,899.18			45,136
I. TOTAL EXPENDITURES	7,087.09	13,203.65			12,966.32 14,866
					46,756.35 \$60,000

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COST ANALYSIS OF RESEARCH PROJECTS

CONTRACT 30-45-0210607-232

DATE THIS REPORT July 1, 1978

PROJECT TITLE NASA Contract NAS8-26742

THROUGH July 31, 1978

	EXPENDITURES THIS MONTH	EXPENDITURES TO DATE	OUTSTANDING COMMITMENTS	FREE BALANCE	TOTAL PROPOSED BUDGET
A. PERSONNEL SERVICES					\$22,806
(1) Professional					6,350
(2) Graduate Assistants					1,681
(3) Undergraduate Assistants					
(4) Technical					
(5) TOTAL PERSONNEL SERVICES	6,029.86	13,634.05		10,471.92	
B. MATERIALS AND SUPPLIES	21.29	483.52		2,366.45	2,850
C. EQUIPMENT					
D. TRAVEL		123.44		2,429.55	2,553
E. EMPLOYEE BENEFITS		1,023.85		2,671.15	3,695
F. OTHER (Specify) Computer Service				3,000.00	3,000
G. TOTAL DIRECT EXPENDITURES		90.75			45,134
H. INDIRECT COST 45.3% of A(5)				12,956.82	14,396
I. TOTAL EXPENDITURES	4,051.15	17,254.80		42,745.20	46,100

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COST ANALYSIS OF RESEARCH PROJECTS

CONTRACT 30-45-0210607-232

PROJECT TITLE FAS/GRANT NO. 26749

DATE THIS REPORT August 1, 1978

THROUGH

August 31

1978

	EXPENDITURES THIS MONTH	EXPENDITURES TO DATE	OUTSTANDING COMMITMENTS	FEE BALANCE	TOTAL PROPOSED BUDGET
A. PERSONNEL SERVICES					
(1) Professional					\$22,836
(2) Graduate Assistants					8,550
(3) Undergraduate Assistants					1,650
(4) Technical					
(5) TOTAL PERSONNEL SERVICES	2,743.23	16,377.29		16,658.71	33,036
B. MATERIALS AND SUPPLIES					
3. 269.83		753.35		2,096.65	2,850
C. EQUIPMENT					
D. TRAVEL		123.44		2,429.56	2,553
E. EMPLOYEE BENEFITS		1,023.85		2,671.13	3,625
F. OTHER (Specify) Computer Service				3,000.00	3,000
COMMUNICATIONS		90.75		- 90.75	
G. TOTAL DIRECT EXPENDITURES					45,134
H. INDIRECT COST 45% of A(5)	3,016.13	4,915.31		9,930.69	14,855
I. TOTAL EXPENDITURES	6,029.19	23,283.99		36,716.01	\$61,000

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